

IN THE SPECIFICATION:

Please amend paragraph [0004] as follows:

[0004] The individual semiconductor devices may then be packaged. Along with the trend in the semiconductor industry to decrease semiconductor device size and increase the density of structures of semiconductor devices, package sizes are also ~~ever-decreasing, ever-decreasing~~. One type of semiconductor device package, the so-called “chip-scale package” or “chip-sized package” (“CSP”), consumes about the same amount of real estate upon a substrate as the bare semiconductor device itself. Such chip-scale packages typically include a carrier substrate having roughly the same surface area as the semiconductor device itself. As the carrier substrate of such chip-scale packages is small, electrical connections between the semiconductor device and the carrier substrate are often made by flip-chip-type bonds or tape-automated bonding (“TAB”). Due to the typical use of a carrier substrate that has a different coefficient of thermal expansion than the semiconductor substrate of the semiconductor device, these types of bonds may fail during operation of the semiconductor device.

Please amend paragraph [0007] as follows:

[0007] Accordingly, there is a need for a semiconductor packaging process that facilitates testing, probing, and burn-in of semiconductor devices without requiring the alignment of individual semiconductor devices and by which a plurality of reliable ~~chip-scale~~ chip-scale packages may be substantially simultaneously assembled. An efficient chip-scale packaging process with a reduced incidence of semiconductor device failure is also needed. There is a further need for chip-scale packaged semiconductor devices that consume about the same amount of real estate as the semiconductor devices thereof and that withstand repeated exposure to the operating conditions of the semiconductor device.

Please amend paragraph [0021] as follows:

[0021] Contact pads comprising under-bump metallurgy (“UBM”) or ~~ball-limiting~~ ball-limiting metallurgy (“BLM”), which are referred to herein as contacts for

simplicity, may be fabricated on the back side of the substrate wafer. Preferably, each of these contacts correspond to and communicate with a via of the carrier substrate or substrate wafer. The contacts may be fabricated by known processes, such as by known metallization, masking, and etching processes. A conductive bump, such as a solder bump or a solder ball, may be disposed on each of the contacts by known processes.

Please amend paragraph [0040] as follows:

[0040] With reference to FIG. 1, a carrier substrate 10, which is also referred to herein as a semiconductor substrate or simply as a carrier, is illustrated. Carrier substrate 10 is a substantially planar structure that may be fabricated from a semiconductor material, such as silicon. An array of apertures 12-~~are~~-is defined through carrier substrate 10. Preferably, apertures 12 correspond substantially to the bond pads 16 (see FIG. 2A) of a semiconductor device 14 to be assembled with carrier substrate 10.

Please amend paragraph [0043] as follows:

[0043] Contacts 24, such as the ball-limiting metallurgy structures or ~~under-bump~~ under-bump metallurgy structures known in the art, may be disposed in communication with vias 20 and carried by carrier substrate 10 on or proximate back side 11. If carrier substrate 10 includes any laterally extending conductive traces 22, contacts 24 may be disposed adjacent such conductive traces 22. Referring again to FIG. 2A, contacts 24 that communicate with vias 20 that do not include laterally extending conductive traces 22 may be disposed adjacent such vias 20. A conductive bump 26, such as a solder bump or a solder ball, may be disposed adjacent each contact 24.

Please amend paragraph [0048] as follows:

[0048] Each aperture 12, which is lined with an insulative layer 13, preferably extends substantially through carrier substrate 10. The location of each aperture 12 preferably corresponds substantially to a location of a bond pad 16 (see FIG. 4) of a semiconductor device 14 to be assembled with carrier substrate 10. Apertures 12 may be defined through

carrier substrate substrate 10 by known techniques, such as by known laser machining processes, which are also referred to herein as laser drilling techniques, or by known patterning processes (e.g., masking and etching). Insulative layer 13 may be formed by known processes, such as by employing known oxidation techniques to oxidize the surfaces of apertures 12. Apertures 12 may be defined through carrier substrate 10 and lined with insulative layer 13 either before or after the assembly of carrier substrate 10 with semiconductor device 14.

Please amend paragraph [0065] as follows:

[0065] As shown in FIGs. 8A and 8B, a conductive bump 28' material, such as solder, may be disposed adjacent conductive layer 18'. If layer 18' includes a material that is wettable by the conductive bump 28' material employed, the conductive bump may be drawn into hollow region 19' by capillary action, or "wicking", "wicking."